What is claimed is:

1. A data processor comprising:

a central processing unit;

a data transfer control circuit for controlling data transfers under control of said central processing unit; and

a peripheral circuit for requesting data transfers,

wherein said peripheral circuit selects one of input terminals thereof, processes input data from the selected input terminal, requests the transfer of the processing result, and outputs identification information which permits the identification of the selected input terminal, and

said data transfer control circuit has a destination address register (DAR) with its low-order bits variable according to the identification information from said peripheral circuit.

2. The data processor of claim 1, wherein said peripheral circuit comprises a data register shared for storing the processing results of input data.

3. The data processor of claim 1, wherein said peripheral circuit is an analog-to-digital converter having a converter section and a converter control section for converting analog signals to digital form,

said converter section comprising:

a plurality of analog input channels; and

a conversion data register shared for storing the

conversion results of input signals from said plurality of analog input channels,

said converter control section requesting the data transfer of the conversion results stored in said conversion data register and outputting code information which permits the identification of analog input channels corresponding to said conversion results.

4. The data processor of claim 3, wherein said converter section further comprises an analog multiplexer for selecting one of said plurality of analog input channels, and converts an analog signal from the analog input channel selected by said analog multiplexer to digital form in a successive approximation procedure.

5. The data processor of claim 4, wherein said converter control section comprises a channel-select register for holding selection information which allows said multiplexer to select one of said plurality of analog input channels, and outputs the selection information held by said channel-select register as said code information.

6. The data processor of claim 5, wherein said converter control section comprises a computing element for incrementing the value of said channel-select register.

7. The data processor of claim 1, wherein said data transfer control circuit is a circuit for controlling data transfers by loading transfer control conditions from a memory in

response to data transfer requests, and so arranged that address information set in a destination address register thereof according to the loaded transfer control conditions can be overwritten with said identification information.

8. The data processor of claim 1, wherein said data transfer control circuit is a circuit for controlling data transfers according to transfer control conditions previously set by said central processing unit, and so arranged that address information set in a destination address register as transfer control conditions can be overwritten with said identification information.

9. The data processor of claim 1, further comprising a RAM which can be addressed using address information held by said destination address register.

10. The data processor of claim 9, said data processor is formed into a single semiconductor chip.

11. A data processor comprising:

a central processing unit;

a data transfer control circuit for controlling data transfers under control of said central processing unit; and

a peripheral circuit for requesting data transfers,

wherein said peripheral circuit performs processing in response to the occurrence of an event to be dealt with, requests the transfer of the processing result, and outputs identification information which permits the identification

of the event occurrence corresponding to the processing result, and

said data transfer control circuit comprises a destination address register with its low-order bits variable according to identification information from said peripheral circuit.

12. The data processor of claim 11, wherein said peripheral circuit comprises a data register shared for storing the processing results thereof each time said event occurs.

13. The data processor of claim 11, wherein said peripheral circuit has a counter section and a counter control section,

said counter section comprises a counting element and a data register for storing the counted values of said counting element, and

said counter control section stores the counted values of said counting element in said data register in response to the notice of event occurrence from event input channels to be dealt with, requests the transfers of the counted values stored in said data register, and outputs code information which enables the event input channel with such a change to be discriminated from other event input channels as said identification information.

14. The data processor of claim 13, wherein said data register is an input capture register shared by said event input channels.

15. The data processor of claim 11, wherein said data transfer

control circuit is a circuit for controlling data transfers by loading transfer control conditions from a memory in response to data transfer requests, and so arranged that address information set in said destination address register can be overwritten with said identification information according to the loaded transfer control conditions.

16. The data processor of claim 11, wherein said data transfer control circuit is a circuit for controlling data transfers according to transfer control conditions previously set by said central processing unit, and so arranged that address information set as transfer control conditions in said destination address register can be overwritten with said identification information.

17. The data processor of claim 11, further comprising a RAM that can be addressed using address information held by said destination address register.

18. The data processor of claim 17, said data processor is formed into a single semiconductor chip.

19. A data processor comprising:

a central processing unit;

a data transfer control circuit for controlling data transfers under control of said central processing unit; and

a peripheral circuit for requesting data transfers,

wherein said peripheral circuit selects one of data input channels thereof, performs a predetermined processing for

input data from the selected data input channel, requests the transfer of the processing result, and outputs identification information which permits the identification of the data input channel corresponding to the processing result,

said data transfer control circuit has a source address register and a destination address register with their low-order bits variable according to the identification information from said peripheral circuit.

20. The data processor of claim 19, wherein said peripheral circuit has a plurality of data registers for storing the processing results of input data from said data input channels.

21. A data processor comprising:

a central processing unit;

a data transfer control circuit for controlling data transfers under control of said central processing unit; and

a peripheral circuit for requesting data transfers,

wherein said peripheral circuit performs processing in response to the notice of event occurrence from event input channels to be dealt with, requests the transfer of the processing result, and outputs identification information which permits the identification of the event input channel corresponding to the processing result,

said data transfer control circuit has a source address register and a destination address register with their low-order bits variable according to the identification

information from said peripheral circuit.

22. The data processor of claim 21, wherein said peripheral circuit has a plurality of data registers for storing the processing results in response to said event occurrence notice.